FUSE DEMONSTRATOR DOCUMENT

AE23290

Digital Audio Hi-Fi System

FPGA technology improves performance at lower cost

Company: DPA Digital Ltd

TTN: University of Glamorgan Commercial Services (UGCS) Ltd

January 1998

Version 3.0

Abstract

DPA Digital Ltd. is small company of 5 employees and an annual sales revenues of approximately 250 KECU per annum. The company is involved in the design, manufacturing and marketing of a range of high-end hi-fi equipment for the domestic consumer market.

The objective of this application experiment (AE) is to improve the company's existing reference Digital to Analogue Converter (DAC), the PDM1024, by utilising FPGA technology. The current implementation of this and all the other company products was based on standard and discrete analogue and digital components. The company did not have any expertise in electronic development using FPGA technology or higher. In addition, the company did not have experience in the design of complex digital systems.

The use of FPGA devices has enabled the company to improve its existing DAC by incorporating its proprietary patent-pending Pulse Array Modulation (PAM) technique into the design of the noise shaper of the DAC. This has enabled the company to produce a much improved product at reduced manufacturing costs.

The total costs of the AE were 28,000 ECU. The development programme was started in October 1996, and was completed in 9 months. The projected improvements in the company's sales of the DAC range of products will ensure a payback period of 13 months. The anticipated return on investment (ROI) over the product life, expected to be 4 years, is 650%

Prior to this application experiment, the company had a strong perception that the introduction of FPGA technology, and other advanced microelectronics technologies, would be a high risk venture. Therefore, it was unable to improve its DAC range and adopt a suitable technology to integrate the complex digital circuits. The experience gained during the AE has proved the viability of the FPGA solution and the low risks associated with the adoption of this technology. The company is currently planning to utilise FPGA technology into its other audio products to maximise the impact of this technology on the company's business.

This application experiment and its results will be of interest to companies involved in the design and manufacture of specialist consumer electronic products, especially audio and entertainment systems, and small enterprises engaged in the design and manufacture of specialist equipment for niche markets.

1. Company name and address

DPA Digital Ltd.
81 Dobbins Road
Barry
CF63 2NP
UK

2. Company size

DPA Digital has an annual sales revenue of approximately 250 KECU. The total number of employees in the company is 5. DPA Digital has its own in-house design and manufacturing capability. The company has a proven track record in developing its innovative designs. Four of the company's employees are involved in electronics, and these individuals are involved in design (1 person), production and assembly (2), and production testing (1).

3. Company business description

DPA Digital designs, manufactures and markets a range of high end audio electronic equipment for the domestic consumer market. The company's products include digital to analogue converters (DACs), audio power amplifiers, pre-amplifiers, CD players, drives, mains filters, cables and other accessories.

4. Company markets and competitive position at the start of the AE

DPA Digital operates in a specialist niche market selling a range of high end and high quality audio electronic equipment for the domestic consumer market. The company currently achieves less than 1% market share of any market it addresses.

Its largest markets are the UK, Germany, USA and Taiwan. The company exports 70% of its products with the remainder sold in the UK. The exports are equally shared between Europe and the rest of the world. The company's current share of the UK market is exactly 1%, and is less than 1% of the world wide specialist audio DAC market.

The world wide market size for the sale of high end hi-fi audio equipment has been estimated at over $300m in sales turnover per annum. This equates to sales of over 100k units per year.

DPA Digital has many different markets each with different principal competitors. The company sells to virtually all European countries, the Far East, Australia, New Zealand, and North America.

In Europe, the main competitors are other British companies. These competitors include Linn, Name, Audion Lab and Meridian.

For the rest of the world, particularly the USA, the main competitors are American. The major competitors in these markets include Krell Digital (USA), Theta (USA), Audio Research (USA), Mark Levenson (USA), and Esoteric (Japan).

All of these companies have annual sales turnovers in the range 5 MECU to 20MECU, and are therefore significantly larger than DPA Digital. Competition at this high end audio equipment market is determined largely by technical specification, and sales occur to knowledgeable end users. Sales are achieved via specialist dealers and directly to customers. Important direct marketing routes include specialist trade shows, HI FI review journals and advertising in this literature.

Technical performance can be related to the linearity and resolution provided by the DAC systems provided by these companies. The competitors DAC products generally rely on the use of commercially available, high specification digital to analogue converter devices. The specification for these devices is generally for 20 bit resolution but typically 16 to 18 bit linearity. The company's current product's performance is at the top end of this range.

However, the company's biggest problem is in penetrating the North American market. The competition is fierce, and is provided by large American companies. To penetrate this market, the company needs a massive lead in technology and performance to overcome the competitors who are well established with strong brand names and loyalty. The product development undertaken in the FUSE application experiment will result in a 24 bit linearity performance, allowing this performance lead to be achieved.

5. Product to be improved and its industrial sectors

Product: The PDM1024 Digital to Analogue Converter (DAC).

Product industry sector: Prodcom code 32 (Audio-visual consumer electronics).

The product that was improved during the AE is the company's reference DAC, the PDM1024. The product is marketed towards the discerning hi-fi user and aimed at the domestic consumer market. It has received several favourable reviews around the world stating that it is the best performing DAC available whilst not being the most expensive.

The PDM1024 has 8 digital inputs:

- Four coaxial.
- Three Toslink.
- One AT&T optical.

It accepts any current digital source from 16 bit 44.1 KHz CD to 24 bit 48 KHz professional standard.

Figure 1 shows a block diagram of the PDM1024. The functions of the main building blocks are as follows:

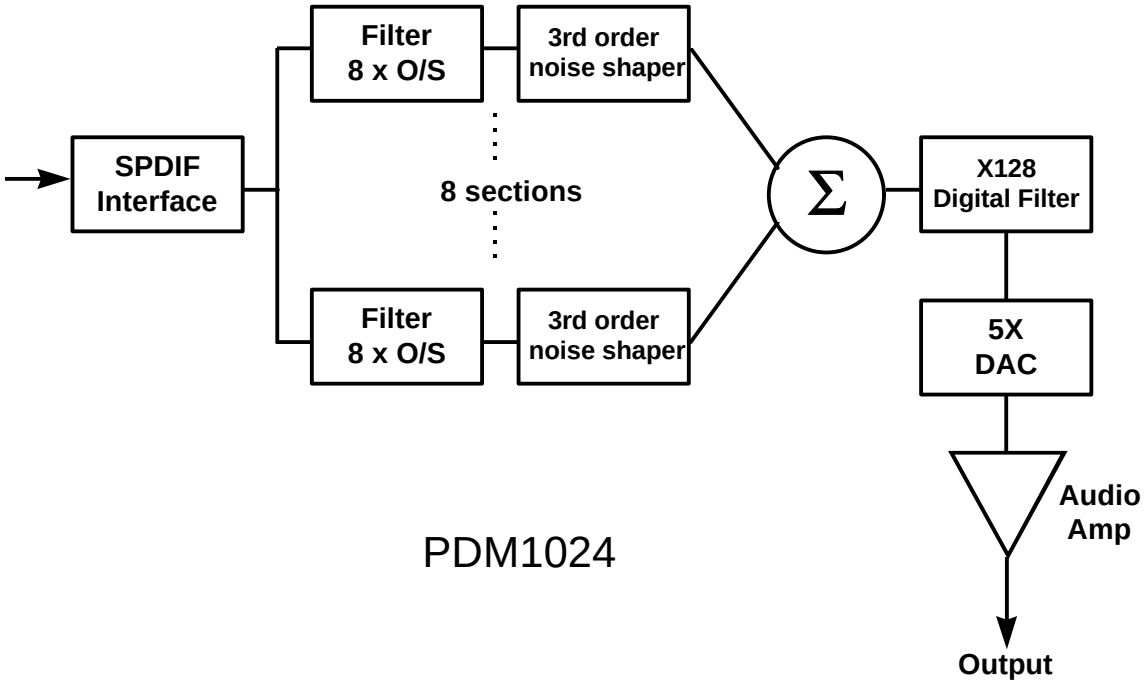

Figure 1 - Block diagram of the existing DAC product, the PDM1024.

- SPDIF interface. This block generates data and clocks for the 8 times over-sampling (OS) filters. The data fed into each filter are marginally different.
- 8 times OS filter. Generates 8 times over-sampled data for the noise shaper.
- Third order noise shaper. Converts the 8 times OS 20 bit data into a 1 bit stream at 192 times.
- Summing and filtering. Each data stream is delayed and then summed in the DX processor. This gives 128 times filtering with a moving average scheme and results in SinX/X comb filter.

- SX DAC. This converts the delayed 1 bit data stream to an analogue form via discrete switched capacitor networks.
- Audio out. Discrete power operational amplifiers are used to buffer the outputs.

The PDM1024 uses the company's proprietary DAC design, the DX128. This converts the 1 bit bit-stream from the noise shapers to analogue, and provides digital filtering of over-sampled images by at least 25 dB. To provide better high frequency resolution of the noise shapers, eight of them are employed, each being fed by its own separately dithered signal.

The PDM1024 suffers from two problem areas:

- High frequency resolution limitations.
- Out of band correlated noise generating inter-modulation distortion in the output operational amplifiers and subsequent audio stages.

Although the parallel arrangement of the noise shapers improves the high frequency resolution, improvements are needed to provide the performance levels required to significantly out perform competitor products..

The second problem area, correlated out of band noise, comes from three sources, which are:

- Over-sampling images at 8, 16, 24 and other multiples of the sampling rate. This is reduced by a minimum of 25 dB within the PDM1024's DX128 DAC.
- Noise shaper noise. With standard single bit noise shapers, correlated out of band noise is at -20 dB from 1 MHz up to the master clock frequency.
- Dither noise. High frequency dither is added in noise shapers to improve low-level resolution and fundamental linearity. This dither is present at the noise shapers output and is modulated by the wanted signal.

The out of band noise creates in band inter-modulation products from the non-linearity in the output operational amplifiers. This causes noise floor modulation that is audible as grain or hardness in the treble frequency band.

The current implementation of the PDM1024 utilises standard analogue and digital components. Most of the devices used are surface-mounted.

6. Description of the technical product improvements

To overcome the limitations of the PDM1024, and the company's other DAC products, a major improvement in the digital processing approach was required. This was achieved during the AE by improving the noise shaper performance through the use of the company's patent pending Pulse Array Modulation (PAM) technique. To implement this processing technique, several FPGA devices were utilised to integrate the digital sections of the product. The resulting improved equivalent of the PDM 1024 is the SX512, which has a design complexity of 50K gates and utilises 9 FPGA devices.

The digital circuitry implemented within the FPGA devices performs three major functions including:

1. Digital filtering and addition of dither. This part of the design includes an input interfacing stage, several up-sampling stages each with a moving average filter, and a dither addition stage with -2.05 dB attenuation to prevent overloading the noise shaper.

2. Fourth order noise shaper. This section takes the 24 bit output from the first section over-sampled at 256 times and converts it to 256 times 4 bits.
3. Dither subtraction and generation of pulse array outputs.

The system designed utilised 9 FPGA devices encompassing 4 different functions. The characteristics of these devices are described in table 1.

Function	Number Used	Approximate Gate Count
Pulse Array Modulator	4	2,500 gates
Noise Shaper	2	8,000 gates
Digital Filters	2	8,000 gates
Controller	1	4,000 gates

Table 1 - FPGA device functionality and complexity.

The final design configuration was a compromise between the availability of device sizes and optimum splitting of the system functionality.

Additionally, analogue and digital sub-assemblies are used to support the digital circuits implemented in the FPGA devices. These include power supply, interfaces, filtering and analogue outputs.

Figure 2 is a block diagram of the improved product. It identifies the major building blocks and shows those implemented within the FPGA devices. Some of the blocks have already been defined in section 6. The blocks in figure 2 are:

- Deltran turbo. The controller circuit, over a period of time, measures where the SPDIF input serial data stream transitions occur. It then selects a suitable clock to re-synchronise the input data. Data is thus, re-synchronised to the master clock without error or jitter.
- SPDIF interface. This takes the SPDIF data and extracts the clocks and serial data. This data is then fed to the controller (CNTR FPGA).
- 8 times filter. This block converts the times 1 and times 2 over-sampled data, interpolates and filters to times 8 over-sampling.
- 24 times OS filter. This block takes the times 8 over-sampled output, over-samples and filters to 192 times. Stop band noise is typically less than 100 dB up to 192 times. Dither and scaling is also applied. The output is 26 bits at 192 over-sampling.
- Fourth order noise shaper. The 192 times 26 bit data are noise shaped to 7 output bits.
- Pulse array modulator (PAM). The 7 bits are fed via opto-isolators to the PAMs. Four devices are used, and 256 elements are created.
- Summing. The PAM elements are summed and filtered by 256 0.1% resistors and capacitors.
- Output operational amplifiers. This block consists of two high performance discrete operational amplifiers. One is for the positive output, whilst the other is for the negative output.

The performance of the improved product has been tested and evaluated. It showed a marked performance improvement over its predecessor the PDM1024, and provided the required 24 bit performance for the frequencies of interest.

Based on the latest prices of the FPGA devices, the overall cost of the improved product is reduced from that of the PDM1024. This shows an additional benefit in the new implementation. It is important to note that cost reduction was not the main objective of the AE. The main objective was to improve the performance of the DAC, and cost reduction was achieved by careful design and planning. The recent drop in the FPGA prices have helped to achieve this significant reduction in the overall cost of the improved product.

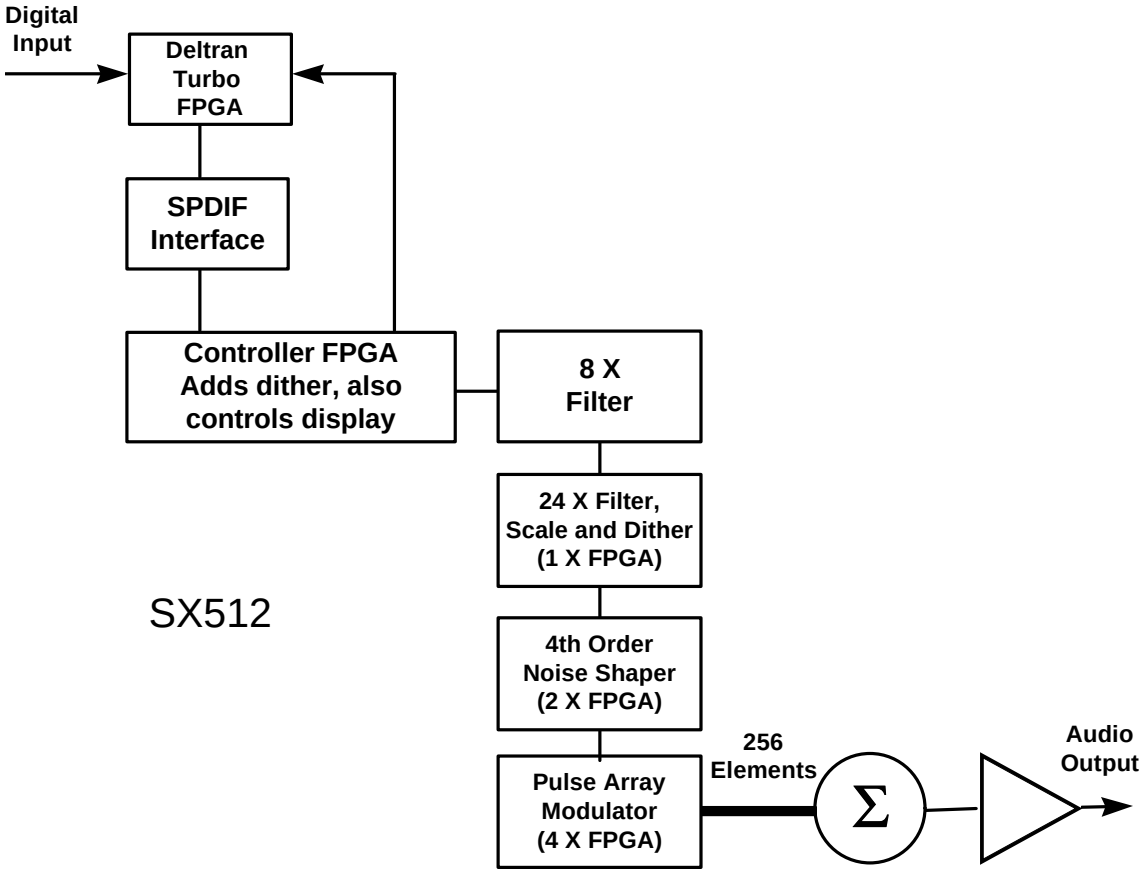

Figure 2 - Block diagram of the improved DAC product, the SX512.

The AE was conducted to improve the PDM1024 and produce its FPGA PAM-based equivalent, the SX512. However, the same design is used in lower product in the same series including, the SX256 and SX128. The latter two devices have less complex circuitry and utilise fewer FPGA devices.

Photograph 1 - Illustration of the Improved Product

7. Choices and rationale for the selected technologies, tools and methodologies

During the feasibility analysis phase and the preparation of the AE proposal, the company in collaboration with its design and training subcontractor conducted an investigation into the various approaches to the implementation of the PAM-based improved product. The technologies considered included:

- **Standard components.** This approach was used in the PDM1024. However, with the complexity of the PAM and associated digital circuitry which was as high as 50K gates for the improved product, the SX512, it is not feasible to use standard devices or even PLDs. Such an approach will result in a very large number of components.
- **Microprocessors and microcontrollers.** These devices were rejected as possible implementation routes because of the high processing speed requirements of the design. It was not possible to identify any microprocessor device which can implement the DAC functions at the required speeds.
- **Digital Signal Processors (DSPs).** Similar to microprocessors, DSPs cannot implement all the required functions of the SX512 due to speed and input / output limitations. However, a DSP can implement part of these functions and additional external logic will still be necessary. Furthermore, high performance DSPs are expensive and some require external support devices. Based on cost, complexity, neatness of the solution, and future upgrade requirements it was decided to reject the use of DSPs.
- **ASIC technology.** ASIC technology is highly suitable for this application. It can implement all the digital functions at the required speeds. In addition, a mixed-signal ASIC can integrate most of the analogue functions in the product. However, the main difficulty with utilising ASIC technology is the high NRE costs, and high unit costs at the volumes required by DPA Digital. The company anticipates an annual production volume of, typically, a hundred items per annum; this is not a viable volume for ASIC manufacture. Furthermore, the company felt that utilising ASIC technology in the first generation of the PAM-based product carries high risk and makes future improvements and upgrades very difficult. This may become a viable option if the market expands to tens of thousands of units. This not expected to be the case for the whole product, but the

company may be able to market PAM-based DAC as an OEM component. In the latter case, it may be necessary to produce the DAC as an ASIC and supply it as an OEM device.

- **FPGA Technology**. FPGA devices offered the best approach to implement the complex digital circuits of the DAC. They offer high gate count, large number of input and outputs, and high speed performance. Furthermore, they offered the company a low risk solution with easy routes for future improvements and upgrades. The cost of FPGAs, though higher than some other implementation routes, but was found to acceptable in relation to selling price of the product. In addition, the key sections of the DAC, mainly the PAM unit, can still be marketed as an FPGA based OEM chip. Therefore it was decided to use this technology in the AE.

In searching for suitable FPGA devices, several technologies and vendors were considered. After careful consideration, only two contenders proved to be suitable for this application. Other similar devices from other vendors did not add any advantages. The two main FPGA device types that were considered in detail were SRAM-based re-configurable devices and anti-fuse one-time programmable (OTP) FPGAs. Anti-fuse FPGAs were selected as, at the time of starting the AE, it provided the following advantages:

- Lower cost.
- Design security.
- A logic block structure that suited the company's requirements.
- Quality of the synthesis and macro generation CAD tools.
- A configuration memory device is not necessary.

The PC-based design system purchased for the application experiment had a Viewlogic schematic capture and simulation tools for design capture and verification. VHDL was not used as a design entry method to reduce the time required to complete the work. In addition, the macro generator tool offered by the CAD system provided an easy to use alternative for generating register transfer level logic structures, which are normally described using VHDL. However, the company intends to adopt VHDL as a means of capturing parts of its future designs and to ensure portability.

The design flow followed standard FPGA development methodology. This included design capture using schematics and the macro generator. Functional simulation was then performed to ensure the correct operation of the algorithms. The designs were then placed and routed and timing simulation is performed to ensure correct operation after routing. The bit stream was then generated for each FPGA device to program the devices.

The first test performed was to compare the simulation results with the mathematical model of the noise shaper. This confirmed the correct functionality of the design. The final tests involved measuring the outputs of the noise shaper and DAC. The company's Audio Precision System One was used for this purpose. This system has a 24 bit generator and the internal notch filter, errors as low as -160 dB can be resolved. This was adequate for the purpose of assessing the unit's real performance.

Subjective testing was also used during the development and final tests. Some key optimisation of the noise shaper algorithm can only be done with subjective testing. In addition, the final listening tests of the completed product verified the expected improvements in sound quality. A blind test sequence was developed to assess the subjective performance in an accurate objective manner.

8. Expertise and Experience in Microelectronics

DPA Digital has experience in high performance analogue and discrete digital audio design and has developed several high performance thick film hybrid circuits. The company's designer has very limited knowledge of digital design before starting the application experiment. The most complicated digital design encountered utilised standard LSI devices and a few gates for glue logic. Therefore, the company did not have any experience in designing large digital circuits or the implementation of complex digital algorithms. The real expertise of the company was in analogue design, coupled with the ability to produce solutions to real problems. The company did not possess any experience in design and development with FPGAs.

The company has its own SMT automation equipment (Dynapert) and all designs are produced with computer-aided design (CAD) tools including CADSTAR for PCB design, and Generic CADD for mechanical design. Automated testing is accomplished with Audio Precision System One.

9. Workplan and rationale

The workplan of the application experiment consisted of the following main stages:

1. *Training*

   This task was conducted during the first two months of the application experiment. The company designer utilised a 40 hour distance learning package provided by the training provider. This enabled the company to become familiar with the concepts of FPGA design methods in a short period of time. In addition, the company received support during this period of the experiment from the training provider and the supplier of the CAD system. Self learning formed a large part of the training period.

2. *Functional and technical specifications*

   This task was completed during the second month of the application experiment and included several iteration to achieve clear functional specifications of the noise shaper algorithms and the technical specifications of the improved DAC, the SX512.

3. *Design and simulation*

   This part of the experiment was conducted during months 3 to 5 of the experiment. It included the design and extensive simulation of the FPGA based sections of the DAC. In addition, the design of the other digital and analogue sections was conducted during this phase of the experiment. During this phase the CAD system supplier and the subcontractor provided support to the company.

4. *Design of PCBs and prototype assembly*

   This task was conducted during months 5 and 6 of the experiment and resulted in the completing the PCB layout design, producing the PCBs and assembling the prototype units.

5. *Prototype testing*

   This task was conducted during months 7 and 8 and was a critical part of the experiment. During this phase extensive functional testing of the prototype was performed to ensure the correct operation of the DAC. The prototype audio performance is also tested during this step of the experiment.

6. Evaluation of test performance and design optimisation

During this task the results from the previous stage were evaluated to compare the actual performance against the expected one, which was based on the mathematical model of the system. The results led to changes in the design of the FPGAs and the analogue sections to optimise the performance of the noise shaper. This task was completed in months 8 and 9. Following the completion of this task preparation for production were completed. This has enabled the company to ship the first improved product to a customer approximately one month after completion of the experiment.

In addition, to the above task, DPA Digital has spent additional effort on technical management of the experiment, reporting and preparation of the dissemination information. The adopted workplan is illustrated in figure 3.

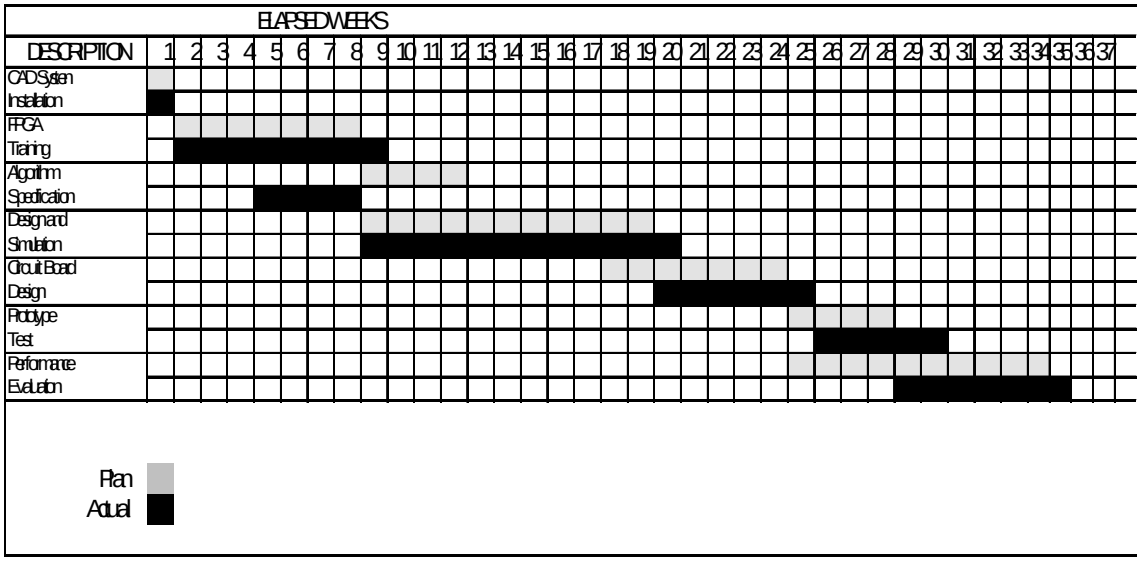

Figure 3 - Actual and Planned Work Programme

The work plan adopted deviated from that planned mainly by the advanced phasing of the algorithm specification to coincide with the final stage of company self training. This allowed the company engineer to undertake the design and simulation task in isolation from the algorithm specification task, thereby allowing the engineer to fully concentrate on the use of design entry and simulation tools for the system functional simulation. The majority of the other tasks were conducted as planned. However, the prototype test and functional evaluation tasks planned to occur in parallel largely operated in series; this reflected an impractical initial plan and the actual plan is more advisable. The resource requirements for the development of initial prototype equipment were as illustrated in table 2.

Tasks	Planned company effort (days)	Actual Company Effort (days)	Subcontractor Costs (KECU)
Engineer Training	20	20	-
Technical Management	20	20	1.0
Functional & Technical Specification	24	25	1.3
FPGA Design & Simulation	68	75	1.3
PCB Design	10	10	1.0
Prototype Testing	28	30	-
Total	170	180	4.6

Table 2 - Resource Requirements for the Application Experiment

The application experiment was completed on time and within the budget. However, the design effort was greater than expected due to the several new design concepts which were introduced during the experiment. This extended the design and simulation times required for the application experiment.

10. Subcontractor information

The company elected not to employ a design subcontractor to support its design and evaluation work. This very unusual approach was adopted because the company considered that the problems of identifying a subcontractor with the capability to appreciate the specialist audio knowledge required for product development in this product area combined with high levels of experience in FPGA development were low. The company therefore decided to conduct the design and evaluation work with the safeguard of specialist support in the areas of FPGA device methodologies and the use of the selected CAD system. As a result the company conducted all the work on its own, but with some limited support from these two sources.

The characteristics of the subcontractors selected to support the design programme are as follows:

Training Provider: A small training company with no allegiance to any specific vendor of FPGA devices was selected. The training supplier selected was able to provide training in both FPGA technologies reviewed, and had previous experience in the design of FPGA based products. As a consequence the training supplier could provide formal training courses, on going tuturial style training materials, and specific advice at various stages of the design activity.

CAD System Provider: The company carefully identified a CAD system supplier with detailed operational knowledge of the selected tools, and with a willingness to provide on-site support during the initial use of the system. These services were identified at the time of purchase.

This application experiment demonstrates that some companies have the capability of conducting design and development with FPGA technology, once they have started

overcoming their barriers and completed a training course, even if the training is self-directed. However, the on-going support of subcontractors ensures this process is managed much more smoothly than would otherwise result.

11. Barriers perceived by the company in the first use of the AE technology

DPA Digital have a clear understanding of its market and its competitors. The company realised that its existing range of high-quality audio products, especially its PDM DAC range, will eventually come to the end of their lives and demand will drop as a result of the increased competition. The company have also realised that the best approach to improve its competitiveness is to improve the performance of its products with more advanced technologies. As a result DPA Digital, developed its proprietary Pulse Array Modulation (PAM) technique for use in the noise shaper of the DAC. However, this developed remained conceptual and it was difficult to realise using standard devices due to the complexity of the required digital circuits.

The company knew of the existence of FPGA and ASIC technologies and their suitability to integrate complex digital circuits. Due to the small volume of production, the company was informed by various sources that ASIC technology is not cost-effective, and that using FPGAs is a better approach. However, the main barrier that faced the company was the perception that introducing FPGA technology into the company would be a very high risk venture. The reasons for this perception are:

- Lack of sufficient knowledge on the real cost of ownership of FPGA technology.
- Limited knowledge in the design of complex digital systems. This knowledge deficiency did not allow the company to assess the real risks involved in improving its DAC product and resulted in a very conservative estimate of these risks.
- Limited company resources, which meant that the company was not able to dedicate staff to conduct the development work whilst conducting their normal duties of manufacturing, marketing and sales. Therefore, if the company's attempts in introducing FPGA technology were not successful, the impact on its turnover would have been serious.

Therefore, the FUSE support offered the company the opportunity to overcome these barriers and conduct the development with increased confidence.

12. Steps taken to overcome the barriers and arrive at an improved product

Prior to the start of the application experiment, the company made contact with its subcontractor and the TTN to discuss the available routes to implement the improvements in the DAC product.

Out of all the considered options, anti-fuse FPGA technology proved to be the optimum solution. The training supplier supported the company in analysing its requirement and selecting suitable FPGA vendors and CAD tools. This work and the feasibility analysis and the support provided by the TTN helped it to overcome part of its main barriers to adopting FPGA technology. At that stage the company started to understand that the its perception of high risk is real in general terms, because the technology is widely acknowledged as low risk.

However, the perception of high risk is also related to the circumstances of the company in terms of capabilities, resources and market position. The company managed to overcome the barriers associated with the lack of knowledge at an early stage in the application experiment through the training programme and the support it received from the training provider and the

FPGA CAD tools supplier. The training and design phases of the application experiment allowed the company to change its view of the risk associated with the technology, and provided it with a realistic approach to assessing the implications of this type of product improvement.

At the end of this application experiment DPA Digital, has reached a stage were it has overcome the fear of technology that it had prior to the experiment. It is currently considering other more advanced technologies such as DSP and ASICs. The effect of the application experiment on the company was to allow it to assess the viability of technology solutions in a realistic fashion.

13. Knowledge and experience acquired

Prior to this application experiment, DPA digital did not have any expertise in complex digital design. The company did not have any experience in design with programmable logic and FPGAs. This included technical and project management of projects with this level of digital circuit complexity. Its PAM technique was merely a theoretical algorithm which was not proven due to the inability of the company to realise it with standard digital components.

As a result of conducting this application experiment has acquired knowledge and developed expertise in the following areas:

- Technical management of FPGA based projects, including the ability to develop viable workplans and accurate cost estimates.
- Selection of FPGA architectures and devices.
- Design methods of complex digital systems.
- FPGA design methods including the use of front-end and back-end CAD tools.
- Implementation of complex algorithms using FPGAs.
- Simulation techniques of digital systems, especially FPGA devices.
- Test and evaluation methods of FPGA based systems.

14. Lessons learned

There were many important lessons learned by DPA Digital in conducting this application experiment. These lessons includes, technology, design and planning issues. Amongst the important lessons were:

- Training and initial design. The FPGA training and design work consumed more effort than expected, as new things often do. Although the elapsed time limits were met, more time was involved than expected. The lesson learned from this is that when planning for activities relating to the adoption of a new microelectronics technology, such as FPGAs, the initial estimated effort should be multiplied by a factor of 1.2 to 2 times to get a realistic estimate.
- DPA Digital learned an important lesson that the risk associated with programmable technologies such as PLDs and FPGAs is relatively low due to their flexibility and programmability. The complexity of the FPGA design tools can be overcome by training and making the appropriate effort by the company. The experiment also shows that a company can acquire this technology without any substantial input from a design subcontractor.

- The experience of DPA Digital has shown that extensive simulation is of vital importance to the success of the FPGA design cycle. However, simulation at the last stages must be conducted with real data to enable proper evaluation of the output data under all conditions. The company used large amounts of real data for this purpose. This has enabled the detection of errors which would have been impossible to detect by simulating artificial data. This process took the same time as the schematic entry part of the design and enabled the designer to locate a serious fault with the controller FPGA.
- The results of the experiment have demonstrated that implementing complex algorithms with multiple FPGA devices can still be a cost effective option in certain high-end applications. The improved DAC costs less than its predecessor to manufacture although it contains 9 FPGA devices.
- To ensure that the improved product is launched as early as possible, it is essential to consider the issues of industrialisation very early in the design cycle. This approach has enabled DPA Digital to ship its first improved DAC shortly after completing the experiment.

15. Resulting product, its industrialisation and internal replication

The company started considering the industrialisation of the product during the progress of the application experiment. This approach was very important to ensure that the product can be launched as early as possible. The company has realised that maintaining a short time to market is one of the main reasons of success.

Therefore, the development process took into account the specification of the final product that will be released on completion of the experiment. This required a parallel development process to ensure that the analogue and digital electronic circuits of the DAC are developed while the FPGAs are being designed. In addition, the PCB and metal case was also designed.

Furthermore, the company conducted the necessary marketing activities to promote the product, including the preparation of a product brochure and attendance of trade exhibitions.

On completion of the application experiment and the success of the final tests, the company was ready to launch the product in prototype form. The manufacturing process of this product did not require any modifications to the company's process which is used with its existing products. The manufacturing of the PCB and enclosure manufacturing is subcontracted, whilst the assembly and functional testing is conducted by the company.

The company has already applied for a patent on the PAM technique used to produce the noise shaper in the DAC.

The FPGA technology adopted in this application experiment is already planned to be used across a wider range of DACs and other similar audio products in the company's range. The company aims to replace all its digital product range with FPGA based pulse arrays. These can be considered as internal replication projects within the company, and as such are a testament to the success of this AE carried out by DPA Digital. Amongst the products that will benefit from the utilisation of FPGA technology are the Renaissance Integrated CD Player and the Enlightenment Drive.

The company is also planning to market the FPGA device that implements the pulse array algorithm of the DAC as an OEM component. If sufficient demand is generated and sales increase significantly, the company will consider migrating to ASIC technology.

The confidence gained by the company during this experiment has allowed it to consider other advanced technologies to improve its competitive position. The experiment has helped DPA Digital to overcome the perception of risk associated with new technology. It is currently negotiating with a major American loudspeaker manufacturer to integrate the DAC developed in this experiment into an ASIC. If the negotiations are successful, DPA Digital will soon acquire ASIC technology and significantly improve its competitiveness.

16. Economic impact and improvement in competitive position

In order to maintain a healthy competitive edge, small, niche companies such as DPA Digital can only really use product quality and or performance to differentiate themselves from their competitors.

In the high-end domestic audio market that DPA Digital operate within, innovation is the key to maintaining a healthy customer base. Due to the nature of this market, many potential customers only hear of new products from smaller manufacturers through reviews in technical and specialist audio journals. Without constantly bringing out new or updated products, companies are unlikely to attract the attention of magazine editors, and as such, demand is soon likely to fall.

Actual and projected sales for the existing DAC product are shown in figure 4.

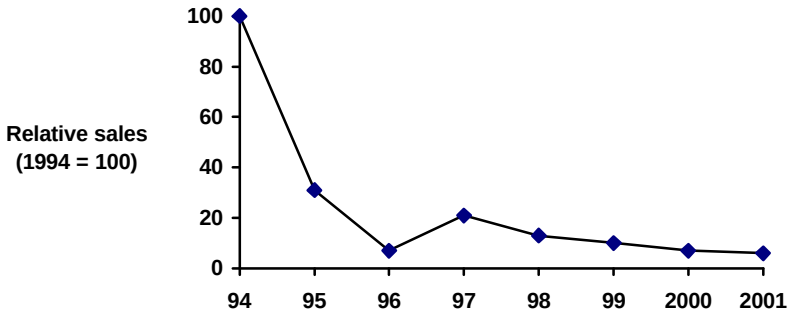

Figure4 - Actual and projected sales of the existing product relative to 1994 sales.

This shows a sharp decline in sales in 1994/95, due to increased competition, followed by a gradual downward trend as the product reaches the end of its useful life. Obviously, without significant improvements, the company's range of DAC products will not be able to compete in the marketplace.

Due to the development of the SX512 product, which incorporates FPGA technology, the fortunes of this product line will be transformed. Even though the AE was only completed part-way through 1997 (to the prototype stage), DPA has already launched the SX512 and have attracted significant sales.

Projections, based on market intelligence, for the SX512, are shown in figure 5. Note that the 1997 figure includes actual sales, rather than mere projections.

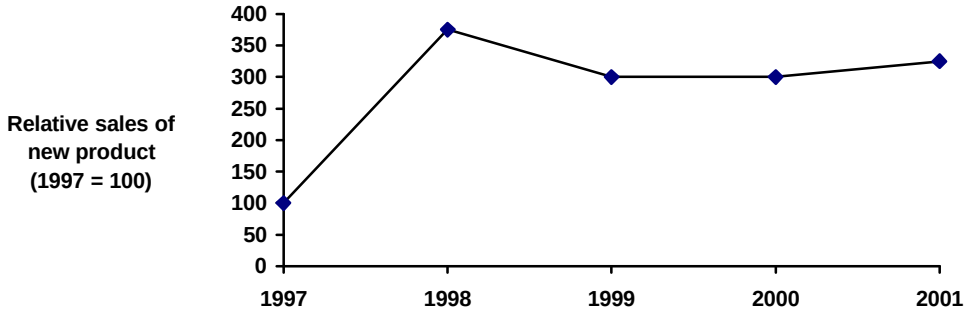

Figure 5 - Projected sales of the existing product.

Due to the launch of the product and the consequential trade and magazine reviews, sales are expected to increase rapidly in 1998. A small fall will follow as the natural penetration level is reached, then as greater market acceptance is gained, sales will start a slow upward trend from 2001.

The relative turnover of the existing and improved products are shown in table 2.

Year	Existing Product	Revised Product
1994	100	-
1995	31	-
1996	37	-
1997	21	36
1998	13	137
1999	10	110
2000	7	110
2001	6	115

Table 2 - Relative increase in sales value compared to existing product (1994 value).

The higher performance and improved quality offered by the new product has meant that the selling price (to the dealer) can be increased by approximately 30%, when compared to the existing product.

The anticipated return on investment (ROI) over the product life, expected to be 4 years, is 650%

The investment in this AE is 28,000 ECU (approximately £20,000). Using the 'net' profit figure for the SX512 revised product, and the projected sales figures for the revised product, the payback period will be 13 months.

17. Target audience for dissemination throughout Europe

This application experiment and its results will have significant benefits to a wide range of European enterprises. The enterprises that should be targeted for disseminating the results of the experiment should include:

- A company in specialist consumer electronic industry segments, especially audio and entertainment system developers.
- Small enterprises engaged in the design and manufacture of specialist equipment for niche markets.
- Small enterprises facing similar barriers to those of DPA Digital. Those include a strong perception of high risk in introducing a more advanced technology, such FPGAs, and the lack of internal resources to spare in terms of management and technical personnel due to the daily demands of the business.
- Companies requiring a similar technological transition to DPA Digital. Such companies normally have a strong background in the design of complex systems which are mainly analogue, but require to introduce high complexity digital circuits which cannot be implemented using standard discrete digital devices.

The main industrial target areas are in industrial sectors identified by Prodcom code 32 and 33.